REMARKS/ARGUMENTS

Status of Application

Claims 1-11 are pending in the subject application. Claims 1, 2, 5, 8/1, 8/2, 8/5, 9 and 10 are rejected under 35 USC § 102 (b) as being anticipated by US Patent No. 4,203,159 (Wanlass). Claims 3, 4, 6, 7, 8/3, 8/4, 8/6, 8/7 and 11 are objected to as being dependent on a rejected base claim but would be allowable if rewritten to include all the limitations of the base claim and any intervening claims. Applicant has, by way of this response, added new claims 12-25.

Amendments to the Specification

Applicant, after reviewing the specification, has amended the specification to correct minor typographical errors, some of which were caused by the electronic filing software. No new matter has been added by way of the amendments.

Rejections under 35 USC § 102

Claims 1, 3, 5, 8/1, 8/2, 8/5, 9 and 10 stand rejected under 35 USC § 102 (b) as being anticipated by Wanlass. Applicant disagrees with the Examiner's rejection. However, to expedite prosecution, Applicant has withdrawn these claims from consideration without prejudice. Applicant therefore submits that the basis of rejection under 35 USC § 102 (b) is moot.

Applicant, by way of this amendment, has added new claims 12-25. Claims 13-25 recite a memory array having first and second ports capable of memory access and refresh operations and a refresh control circuit which allocates refresh operations to either one of the first or second ports which is not occupied with a memory access to reduce contention between refresh and memory access operations.

In contrast, Wanlass only discloses a memory array in which a memory cell is accessed via the main wordline and refreshed via the refresh wordline. As such, refresh operations are performed always through the same transistor or port of the memory cell. See Wanlass col. 6, lines 35-43. The use of a refresh control circuit which allocates a refresh operation to one of the first or second ports which is not occupied by a memory access to reduce contention is nowhere taught or suggested by Wanlass. The remaining references

cited by the Examiner but not relied upon also fail to teach a refresh control circuit which allocates a refresh operation to one of the first or second ports which is not occupied by a memory access to reduce contention. Applicant therefore submits that the newly added claims 13-25 are patentable over the cited art, alone or in combination.

Objection to the Claims

Claims 3, 4, 6, 7, 8/3, 8/4, 8/6, 8/7 and 11 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended claims 3, 4, 6 and 11 to be in independent form and which includes all limitations of the base claim and any intervening claims. Claims 7 and 8 have been amended to be dependent on claim 3, 4 or 6 and newly added claim 12 is dependent on claim 7. Therefore, Applicant submits that claims 3, 4, 6, 7, 8, 11 and 12 are now allowable.

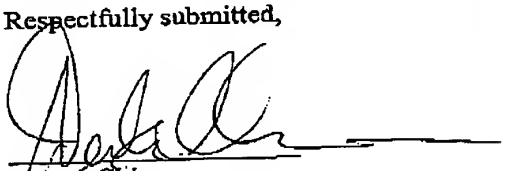
Conclusion

In view of the foregoing, Applicant believes that all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Dated: July 11, 2003

Respectfully submitted,



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